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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/913,688	MORINAGA, TAKEO	
	Examiner	Art Unit	
	TANH Q. NGUYEN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2007 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7-20,25-38,41,43,45,46,48,49 and 51* is/are pending in the application.

4a) Of the above claim(s) *8-18,25-34,36 and 38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,19,20,35,37,41,43,45,46,48,49 and 51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 5, 2007 has been entered.

Claim Objections

2. Claims 1, 2, 19, 20, 35, 37, 45, 48 are objected to because of the following informalities:

"controlling reading said packets" in lines 11-12 of claim 1 should be replaced with --controlling reading of said stored packets-- for clarity and consistency

"a predetermined data amount" in the last line of claim 2 should be replaced with --the predetermined data amount-- to avoid interpretation of "a predetermined data amount" that is different from "a predetermined data amount" recited in the last line of claim 1

"controlling reading said packets" in lines 12-13 of claim 19 should be replaced with --controlling reading of said stored packets-- for clarity and consistency

"a predetermined data amount" in the last line of claim 20 should be replaced with --the predetermined data amount-- to avoid interpretation of "a predetermined data

amount" that is different from "a predetermined data amount" recited in the last line of claim 19

"said packets added said address" in lines 18-19 of claim 35 should be replaced with --said packets having the added address-- for consistency

"to control reading said packets" in lines 11-12 of claim 35 should be replaced with --to control reading of said stored packets-- for clarity and consistency

"to control reading said stored packets" in line 11 of claim 37 should be replaced with --to control reading of said stored packets-- for clarity and consistency

"a predetermined data amount" in the last line of claim 45 should be replaced with --the predetermined data amount-- to avoid interpretation of "a predetermined data amount" that is different from "a predetermined data amount" recited in the last line of claim 35

"a predetermined data amount" in the last line of claim 48 should be replaced with --the predetermined data amount-- to avoid interpretation of "a predetermined data amount" that is different from "a predetermined data amount" recited in the last line of claim 37.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1- 2, 7, 19-20, 35, 37, 41, 43, 45-46, 48-49, 51 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites "a control means" in lines 4-5 and "index adding means, residing outside a central processing unit" in lines 16-17. The claim suggests the central processing unit and the control means to be different entities. The specification does not appear to support the central processing unit and the control means to be different entities. Claims 19, 35, 37 recites limitations that are similar to the limitations of claim 1 above, and are rejected on the same bases.

6. Claims 1- 2, 7, 19-20, 35, 37, 41, 43, 45-46, 48-49, 51 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. See the enablement rejection above.

7. Claims 35, 45-46 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "using a memory control means to control writing of said **extracted** packet", does not reasonably provide enablement for ""using a

memory control means to control writing of said **stored** packet" (see lines 10-11 of claim 35). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

8. Claims 1- 2, 7, 19-20, 35, 37, 41, 43, 45-46, 48-49, 51 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims recite several means (receiving means, control means, extracting means, memory means, memory control means, index adding means, packets transferring control means, address adding means), and it is not clear what element or elements are associated with the respective means. The claim is indefinite because the metes and bounds of the claims cannot be determined without proper association of element or elements with the respective means.

The examiner requests that applicant identifies the element or elements associated with each of the respective means to clarify the scope of the claim and to further the prosecution. A response that does not include identification of element or elements associated with each of the respective means would not overcome the 112 second rejection.

9. The art rejections that follow are based on the examiner's best interpretation of the claims.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-2, 7, 19-20, 35, 37, 41, 43, 45-46, 48-49, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA: pages 1-9 and FIG. 1) in view of Mergard (US 5,881,248).

12. As per claim 1, AAPA teaches an information processing apparatus [a digital broadcast receiving apparatus - FIG. 1] comprising:

receiving means [12, 13, FIG. 1] for receiving a stream constructed by packets of a predetermined format under control of a control means [CPU 1, FIG. 1];

extracting means [21, FIG. 1] for extracting packets from the packets constructing said stream received by said receiving means;

memory means [23, FIG. 1] for storing said extracted packets for recording;

memory control means [28, 1 - FIG. 1] for controlling writing said extracted packets into said memory means, for controlling reading said stored packets from said memory means [page 5, lines 19-23], for issuing a command to prepare transferring [the host CPU executes the issuance of a command to the hard disk, the setting of the transfer start timing - page 8, lines 24-27], and for supplying a start address of a recording means [the host CPU executes the setting of the LBA at every block transfer of recording means 15, FIG. 1 - page 8, lines 24-27];

index adding means [1, 24 - FIG. 1] for adding an address of a sector of a minimum unit of recording on the recording means [the setting of the LBA by the host CPU - page 8, lines 24-27; the address of the minimum unit is expressed by an LBA - page 8, lines 12-13] as an index to said packets read out by said memory control means [LBA being used for address designation to access location on recording means - page 8, lines 1-19], and for outputting said packets having the added address to said recording means [for outputting said packets using the LBA to the recording means];

an arbiter [28, FIG. 1] for mediating said packets extracted by said extracting means and stored in said memory means, and for mediating said packets outputted from said memory means to said index adding means in response to an instruction from said memory control means [page 5, lines 19-23]; and

packets transferring control means [DMA controller - 29, FIG. 1] for permitting write access of said packets outputted from said index adding means to said recording means in accordance with said command from said memory control means [page 8, lines 14-16; page 8, lines 24-26], wherein said packets transferring control means includes an address determining means for starting an address of said recording means when said start address is inputted from said memory control means by counting up said address of memory means each time a cluster of a predetermined amount is transferred [a DMA controller implicitly includes a counter for tracking amount of data transferred as a DMA descriptor/command includes a length of the block transfer].

AAPA does not teach issuing the command before an amount of the packets stored by the memory means reaches a full capacity.

Mergard teaches forming a command when the data amount of the packets stored in the memory means reaches a predetermined capacity in order to prevent the memory from overflowing, the predetermined capacity being less than the full capacity of the memory [col. 7, lines 13-19].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a DMA command when the data amount of the packets stored in the memory means reaches a predetermined capacity, as is taught by Mergard, in order to prevent the memory from overflowing.

AAPA does not teach the index adding means residing outside a central processing unit for adding an address (of a sector of a minimum unit of recording on the recording means) as an index to the packets read out by the memory control means. AAPA essentially does not teach shifting the function of adding an address as an index to packets read out by the memory control means to an index adding means separate from the central processing unit.

Since it was known in the art to shift functions traditionally performed by a central processing unit into dedicated hardware in order to improve overall performance, it would have been obvious to one of ordinary skill in the art at the time the invention was made to shift the function of adding an address as an index to packets read out by the memory control means to a dedicated index adding means (a dedicated hardware separate from the central processing unit) - in order to improve overall system performance.

<u>Alternatively</u>, Dennin teaches a DMA controller integrated with a memory

control means [122, FIG. 1; col. 4, line 66-col. 5, line 1] to allow for high bandwidth transfer from a memory means [112, FIG. 1; col. 5, lines 20-21] to a recording means [106, FIG. 1]. A DMA controller traditionally includes an index adding means (i.e. a counter) for adding an address as an index to packets read out from a memory means for recording to a recording means, and a means for outputting the packets having the added address to the recording means. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a DMA controller with a memory control means, as is suggested by Dennin, in order to allow for high bandwidth transfer from the memory means to the recording means - hence including an index adding means residing outside a central processing unit (because the DMA controller is outside the central processing unit and the DMA controller includes an index adding means).

13. As per claim 2, AAPA teaches the memory means including an input FIFO [23, FIG. 1], and the minimum unit of the recording of the data being a sector of a predetermined data amount [page 8, lines 1-3] - hence said transferring of said packets being made cluster by cluster, the cluster being of a predetermined data amount.

14. As per claims 7, 19-20, AAPA further teach the recording means being a hard disk drive [15, FIG. 1] built in said information processing apparatus [FIG. 1].

15. As per claims 35, 37, the claims generally correspond to claim 1 and are rejected on the same bases.

16. As per claims 41, 43, AAPA teaches said input FIFO sequentially storing said packets for recording and outputting said packets in storing order [page 5, lines 15-17];

said packets transferring control means supplying a start address for the packets to be transferred.

17. As per claims 45-46, 48-49, see the rejections of claims 2 and 41 above.

18. As per claim 51, AAPA teaches said packets transferring control means further including a register for comparison of address of memory [a DMA controller inherently includes a register for comparison of address of memory to determine whether transfer is complete].

Response to Arguments

19. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection and/or not persuasive.

Applicant argues that AAPA does not teach adding an address of a sector of a minimum unit of recording on the recording means as an index to said packets read out by said memory control means. The argument is not persuasive because the CPU sets the address at every transfer (page 8, lines 24-27) - hence adding an address at every transfer; because the address of the minimum unit is expressed by an LBA (page 8, lines 12-13) - hence an address of a sector of a minimum unit of recording on a recording means; and because the LBA is used for address designation to access location on recording means (page 8, lines 1-19) - hence an index to packets read out by the memory control means.

Applicant further argues that AAPA teaches microcontroller 28 monitoring a status of storage in the input FIFO 23 or an output FIFO 25, and controls the reading and writing operations of data in each FIFO, which is quite different from "mediating said

packets outputted from said memory means to said index adding means in response to an instruction from said memory control means" because the memory control means does not receive instructions to mediate from another entity. The argument is not persuasive because the claims do not recite **receiving instructions to mediate** (note that limitations from the specification are not read into the claims although the claims are interpreted in light of the specification, see *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)), and because microcontroller 28 controls the reading and writing operations of data in each FIFO - hence mediating read packets stored in the memory means and write packets output from the memory means in response to a read or write instruction.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TANH Q. NGUYEN whose telephone number is (571)272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TANH Q NGUYEN
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

February 18, 2008

TQN
February 18, 2008